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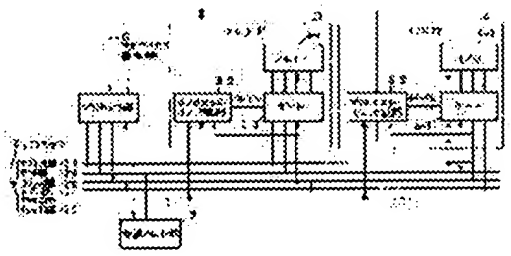
(54) DEVICE FOR PREVENTING ILLEGAL ACCESS

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain an illegal access preventing device in which not only the illegal processing of a processor part but also the writing of illegal data or the illegal operation of an outside device can be prevented.

SOLUTION: A reference memory part 5 stores illegal access detection data. At the time of the access check of a memory part 3 and an I/O part 4, an address or a command or the like is compared with the illegal access detection data, and the permission/inhibition of read and write, access to an unused area, and the normality/abnormality of an address or the like is checked. When the access is normal, a gate 3-3 or 4-3 of the memory part 3 or the I/O part 4 is opened so that the access can be attained. When illegal access is generated, the gate 3-3 or 4-3 is left closed so that the illegal access to the memory part 3 or the I/O part 4 can be inhibited.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] It is the unlawful access arrester of a computer system which the processor section containing a computer controls through a bus line while accessing the address of the first memory or an external device. The second memory which was connected to said bus line and stored beforehand the unlawful access detection data corresponding to said address, The gate circuit inserted between those of said bus line and said first memory, or an external device, Said unlawful access detection data corresponding to the address which said processor section tends to access, and its address are collated. The unlawful access arrester characterized by opening said gate circuit and including an access-control means to control to make said processor section access only when it is detected that it is not unlawful access.
[Claim 2] Said access-control means is an unlawful access arrester according to claim 1 characterized by notifying unlawful access generating to said processor section when it is detected that it is unlawful access.
[Claim 3] Claim 1 to which said unlawful access detection data are characterized by including address error detection data, lead authorization / prohibition status, and light authorization / prohibition status, or an unlawful access arrester given in two.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the unlawful access arrester of a computer system about an unlawful access arrester.
[0002]
[Description of the Prior Art] The processor section (CPU) of a computer system accesses and controls external devices, such as an I/O device and a peripheral device, through a bus line through the memory system and I/O interface which consist of a ROM (read-only memory) and RAM (random access memory). Access from the processor section is performed on the basis of each address. For example, it calls it injustice (address) access to access the address of the memory system which is not used, and the address of an I/O interface to which the peripheral device etc. is not connected. It originates in the bug of software, the noise of pulse nature, etc., and generates, and this unlawful access causes [of the processor section (CPU)] an overrun.
[0003] All the illegal addresses that should be detected beforehand are stored in reference memory at JP,4-21040,A. And when the address actually outputted at the time of access of a device is supervised and unlawful access occurs as compared with the contents of reference memory, interruption is notified to a processor. A processor suspends processing by this interruption. The approach is proposed.
[0004]
[Problem(s) to be Solved by the Invention] When inaccurate data are read by illegal address access in a proposal given in JP,4-21040,A, although unjust processing of a processor is prevented, it cannot be prevented to risk of inaccurate data being written in by illegal address access, and external devices (an I/O device, peripheral device, etc.) carrying out unjust actuation by halt of processing of the processor by detection of unlawful access which interrupts and comes out.
[0005] The purpose of this invention is offering the unlawful access arrester which can prevent not only unjust processing of the processor section by illegal address access but the writing of inaccurate data and unjust actuation of an external device.
[0006]
[Means for Solving the Problem] The processor section containing the computer by this invention minds a bus line. The unlawful access arrester of a computer system controlled while accessing the address of the first memory or an external device The second memory which was connected to said bus line and stored beforehand the unlawful access detection data corresponding to said address, The gate circuit inserted between those of said bus line and said first memory, or an external device, Said unlawful access detection data corresponding to the address which said processor section tends to access, and its address are collated. Only when it is detected that it is not unlawful access, it is characterized by opening said gate circuit and including an access-control means to control to make said processor section access.
[0007] The operation of this invention is as follows. In drawing 1 , the unlawful access detection data in the case of access of the memory section 3 and the I/O section 4 are beforehand stored in the reference

memory section 5. The reference memory section 5 outputs unlawful access detection data according to the address which the processor section 1 outputs.

[0008] The access check of the memory section 3 and the I/O section 4 compares commands, such as the address which accesses the memory section 3 and the I/O section 4, a lead, or a light, etc. with the unlawful access detection data outputted from the reference memory section 5, and checks authorization/prohibition of a lead, authorization/prohibition of a light, access to intact area, normal/abnormalities of the address, etc. When access is normal, the gate 3-3 of the memory section 3 or the I/O section 4 or 4-3 is opened, and access is made possible.

[0009] Since mismatching arises between the address and a command, and unlawful access detection data when unlawful access by the bug of software or the failure on hardware occurs, the gate 3-3 or 4-3 becomes having closed with as, and unlawful access to the memory section 3 or the I/O section 4 is forbidden. Moreover, unlawful access generating is immediately carried out to the processor section 1 notice 6 at the time of unlawful access generating.

[0010]

[Embodiment of the Invention] Below, the example of this invention is explained with reference to a drawing.

[0011] Drawing 1 is the block diagram showing the configuration of a basing-on this invention example. In drawing 1 , the processor section (CPU) 1 consists of microprocessors etc., and controls an entry of data, processing, and an output according to the program (software) stored in the memory section 3.

[0012] The memory section 3 consists of memory 3-1 which consists of semiconductor memory etc., an access error-checking circuit 3-2, and the gate 3-3. By the program which the processor section 1 performs, memory 3-1 stores the data inputted or outputted. The access error-checking circuit 3-2 checks unlawful access (authorization/prohibition of a lead, authorization/prohibition of a light, access to intact area, the normal/abnormalities of the address) to memory 3-1 based on the unlawful access detection data outputted from the reference memory section 5.

[0013] Access to memory 3-1 is attained by directing to always [access forward] open the gate to the gate 3-3. Moreover, by supposing that the gate 3-3 has been closed, access to memory 3-1 is forbidden at the time of unlawful access, and it notifies unlawful access to the processor section 1. The gate 3-3 controls access to memory 3-1 by the control signal from the access error-checking circuit 3-2.

[0014] In the I/O section 4, although constituted by I/O interface 4-1 with external devices (an I/O device, peripheral device, etc.), the access error-checking circuit 4-2, and the gate 4-3, since it is the same as that of the memory section 3, actuation omits explanation of operation fundamentally.

[0015] The reference memory section 5 consists of semiconductor memory etc., and stores unlawful access detection data for the access error-checking circuit 3-2 or 4-2 to detect unlawful access. And the address line 2-1 of a bus line 2 is supervised, and the unlawful access detection data corresponding to the address are outputted to the access error-checking line 2-5.

[0016] A bus line 2 consists of the address line 2-1, the data line 2-2, a command line 2-3, a ready line 2-4, and an access error-checking line 2-5. The address line 2-1 transmits the address signal outputted from the processor section 1. The data line 2-2 transmits the data outputted and inputted from the processor section 1, the memory section 3, and the I/O section 4 to /. A command line 2-3 transmits the predetermined command outputted from the processor section 1.

[0017] In case the ready line 2-4 permits access, it transmits the ready signal outputted from the memory section 3 or the I/O section 4. The access error-checking line 2-5 transmits the unlawful access detection data outputted from the reference memory section 5.

[0018] The memory map of memory 3-1 is shown in drawing 2 . for example, illustration -- like -- access to memory 3-1 -- the work area of 000000H to 00FFFFH(s) -- the program area of 010000H to a lead and light authorization, and 01FFFFH(s) -- as for the intact area of authorization and 030000H to FFFFFFH, in the data-logging area of 020000H to authorization and 02FFFFH(s), only a light considers a lead and a light only for a lead as prohibition.

[0019] As shown in drawing 3 , address error detection data, lead authorization / prohibition status,

and light authorization / prohibition status are set to the reference memory section 5 to all the addresses as unlawful access detection data. In addition, although it is possible to address error detection data to add 1-bit parity or the error correction data of two or more bit configuration, in the case of this example, it explains as what adds 1-bit parity.

[0020] Lead authorization, light authorization, and address parity are first stored in 00FFFFH(s) from 000000H at the reference memory section 5. Data are stored in FFFFFFH from 010000H like the following.

[0021] The data set to the reference memory section 5 are defined as follows. A bit 1 (D0) sets lead authorization / prohibition status, and considers it as 0:authorization and 1:prohibition. A bit 2 (D1) sets light authorization / prohibition status, and considers it as 0:authorization and 1:prohibition. A bit 3 (D3) sets address parity, and sets 0 or 1 to each address.

[0022] The processor section 1 is accessed to the memory section 3 and the I/O section 4 through a bus line 2 after program execution. When the processor section 1 accesses the memory section 3, an address signal is outputted through the address line 2-1 from the processor section 1, and commands, such as data read-out, are outputted to coincidence towards the memory section 3 through a command line 2-3.

[0023] At this time, the reference memory section 5 which is supervising the address line 2-1 outputs the unlawful access detection data corresponding to the address to the memory section 3 through the access error-checking line 2-5. For example, when the processor section 1 accesses the 000000H street (R> drawing 2 2 reference) of the memory section 3 (memory 3-1), the 000000H street (refer to drawing 3) data of the reference memory section 5 are outputted.

[0024] In the memory section 3, the address, the command, and unlawful access detection data which were sent through the address line 2-1, the command line 2-3, and the access error-checking line 2-5 are inputted into the access error-checking circuit 3-2, and unlawful access is checked. This unlawful access check performs the check of address data and commands (a lead, light, etc.) as follows.

[0025] When the processor section 1 performs normal access, the access error-checking circuit 3-2 is judged to be access normal, outputs enabling to the gate 3-3, and outputs data to the data line 2-2 from the address which opens the gate 3-3 and corresponds from memory 3-1. The ready signal which shows access termination is outputted to the processor section 1 through the ready line 2-4 after access termination of the memory section 3. In addition, a ready signal is always set to ON (access termination) on account of explanation.

[0026] When the processor section 1 tends to access the 000000H street (work area) of memory 3-1, According to the failure on hardware etc., abnormalities arise in the address line 2-1 of a bus line 2. The address for example, when it changes to 000001H street As compared with the address parity of unlawful access detection data, a parity error is detected, the gate 3-3 becomes having closed with as, access to memory 3-1 is forbidden, and the access error-checking circuit 3-2 protects data. Unlawful access is notified to coincidence through the notice line 6 of unlawful access at the processor section 1.

[0027] Since, as for the access error-checking circuit 3-2, light authorization / prohibition status of unlawful access detection data is forbidden when the processor section 1 tends to carry out a light by the bug of a program etc. to the 010000H street (program area) to which only the lead of memory 3-1 was permitted, unlawful access is detected. And the gate 3-3 becomes having closed with as, and access to memory 3-1 is forbidden, and protects data. Unlawful access is notified to coincidence through the notice line 6 of unlawful access at the processor section 1.

[0028] Since, as for the access error-checking circuit 3-2, lead authorization / prohibition status of unlawful access detection data is forbidden when the processor section 1 tends to lead the 020000H street (data-logging area) to which only the light of memory 3-1 was permitted by the bug of a program etc., unlawful access is detected. And the gate 3-3 becomes having closed with as, and access to memory 3-1 is forbidden, and protects data. Unlawful access is notified to coincidence through the notice line 6 of unlawful access at the processor section 1.

[0029] Since, as for both the access error-checking circuits 3-2, lead authorization / prohibition status of unlawful access detection data and light authorization / prohibition status are forbidden when the

processor section 1 accesses by the bug of a program etc. to the 030000H street (intact area) of read/write prohibition of memory 3-1, unlawful access is detected. And the gate 3-3 becomes having closed with as, and access to memory 3-1 is forbidden. Unlawful access is notified to coincidence through the notice line 6 of unlawful access at the processor section 1.

[0030] In each case, when unlawful access is notified to the processor section 1, the processor section 1 performs processings (the notice of unlawful access generating to the exterior, notice of processing, etc.) to unlawful access.

[0031] As shown in the timing chart of drawing 4 , Address a is outputted from the processor section 1, and the fixed commands (a memory lead, a memory light, an I/O lead, I/O light, etc.) b are outputted to coincidence. At the time of a data light, Data c are outputted to the data line 2-2 to the memory section 3 or the I/O section 4. Moreover, at the time of a data lead, Data d are outputted to the data line 2-2 from the memory section 3 or the I/O section 4.

[0032] Moreover, the ready signal (ready line 2-4) e is considered as as [ON] on account of explanation. If Address a is outputted from the processor section 1, the unlawful access detection data f will be outputted to the access error-checking line 2-5 from the reference memory 5. notice g When unlawful access occurs, unlawful access is made into the processor section 1 through the notice line 6 of unlawful access.

[0033]

[Effect of the Invention] As explained above, this invention prevents unlawful access to the external instruments (an I/O device, peripheral device, etc.) which detect the abnormalities in the address by the failure on unlawful access (the abnormalities of a lead, abnormalities of a light) resulting from the bug of a program etc., and hardware etc., and lead memory and I/O, and has the effectiveness which can perform prevention of protection of data and unjust actuation of an external instrument.

[Translation done.]